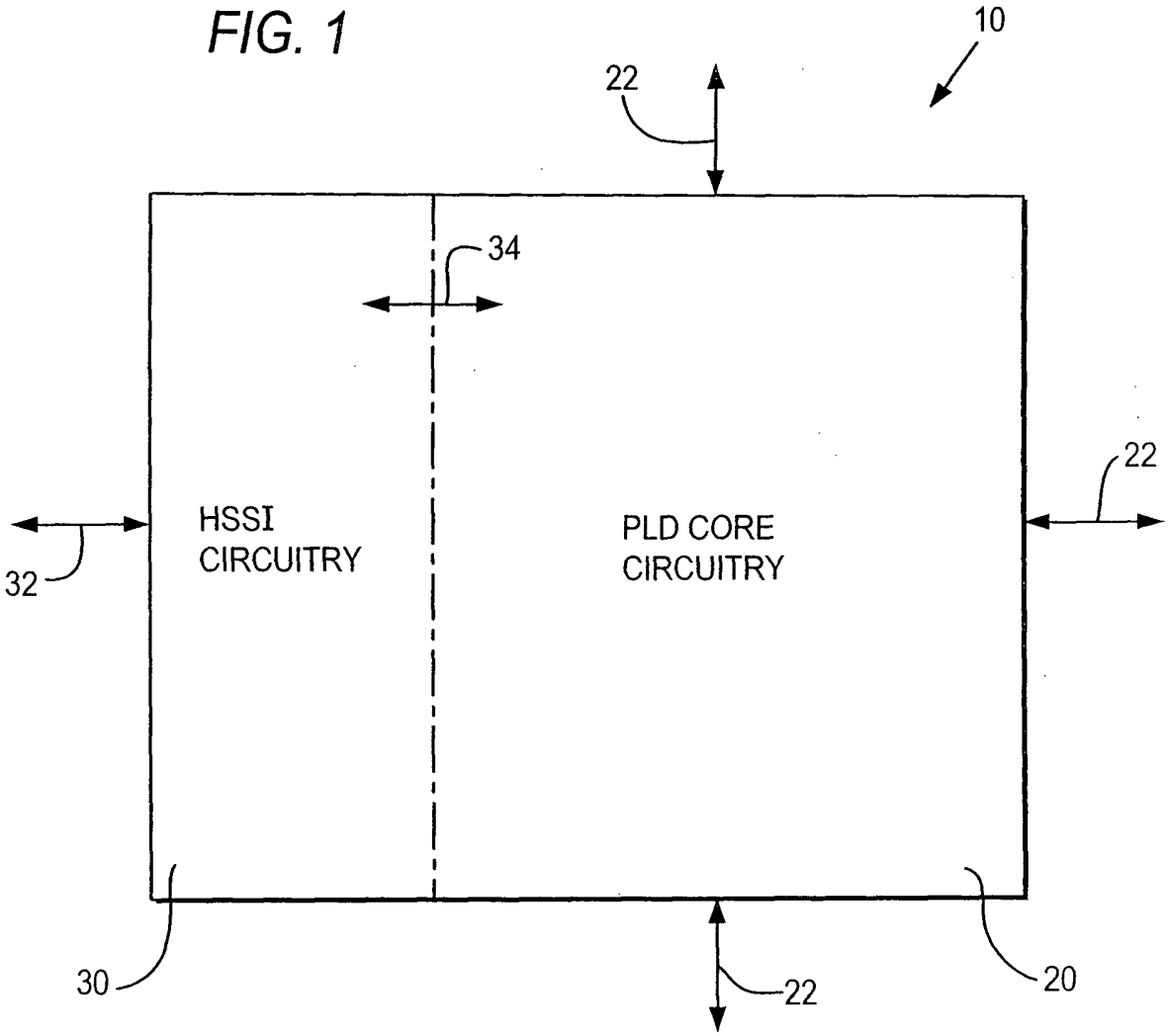
FIG. 1



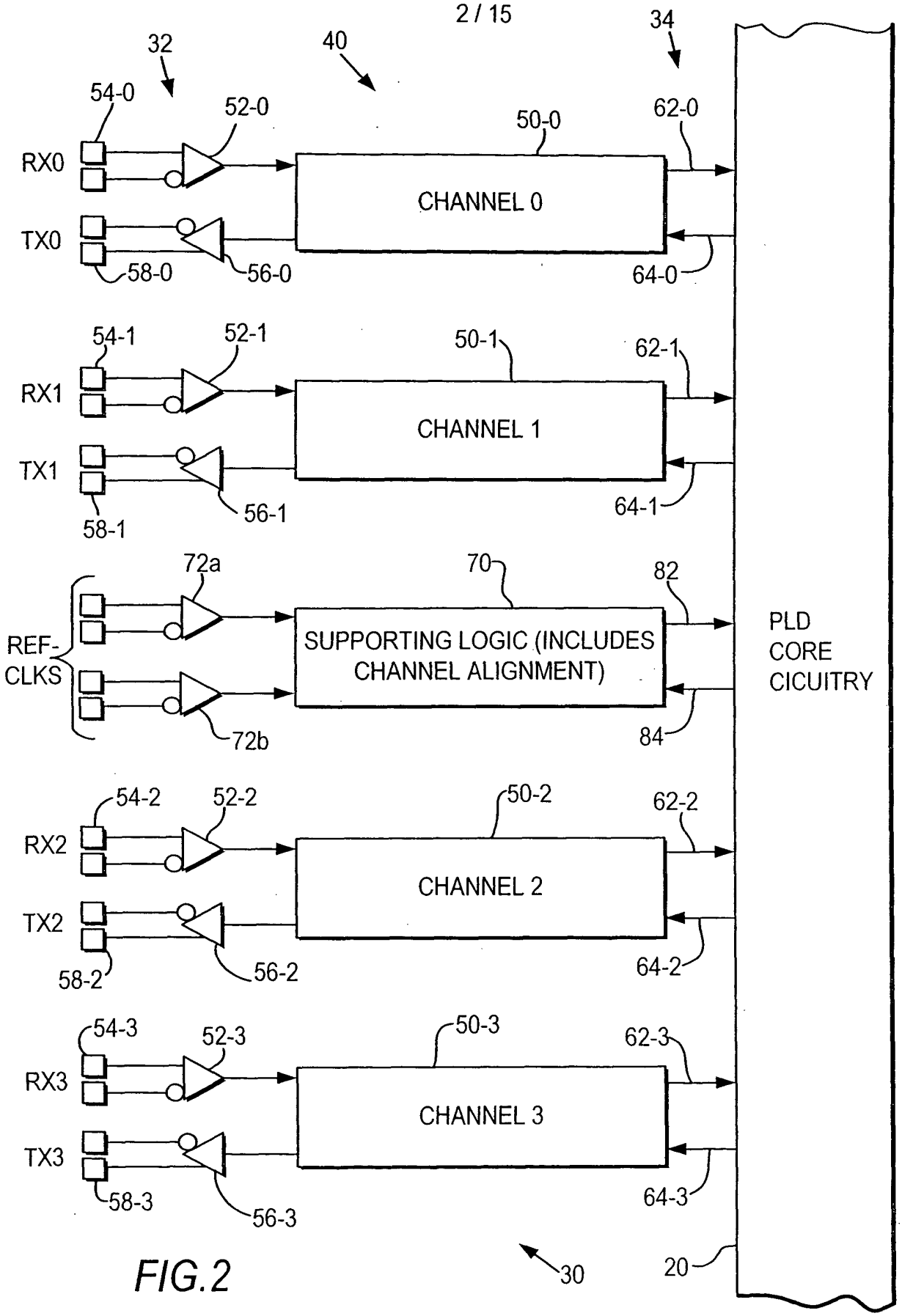

32
40
34
54-0
52-0
50-0
62-0
RX0
CHANNEL 0
TX0
58-0
56-0
64-0
54-1
52-1
50-1
62-1
RX1
CHANNEL 1
TX1
56-1
58-1
64-1
72a
70
82
REF-CLKS
SUPPORTING LOGIC (INCLUDES CHANNEL ALIGNMENT)
72b
84
PLD CORE CICUITRY
54-2
52-2
50-2
62-2
RX2
CHANNEL 2
TX2
58-2
56-2
64-2
54-3
52-3
50-3
62-3
RX3
CHANNEL 3
TX3
58-3
56-3
64-3
30
20

FIG.2

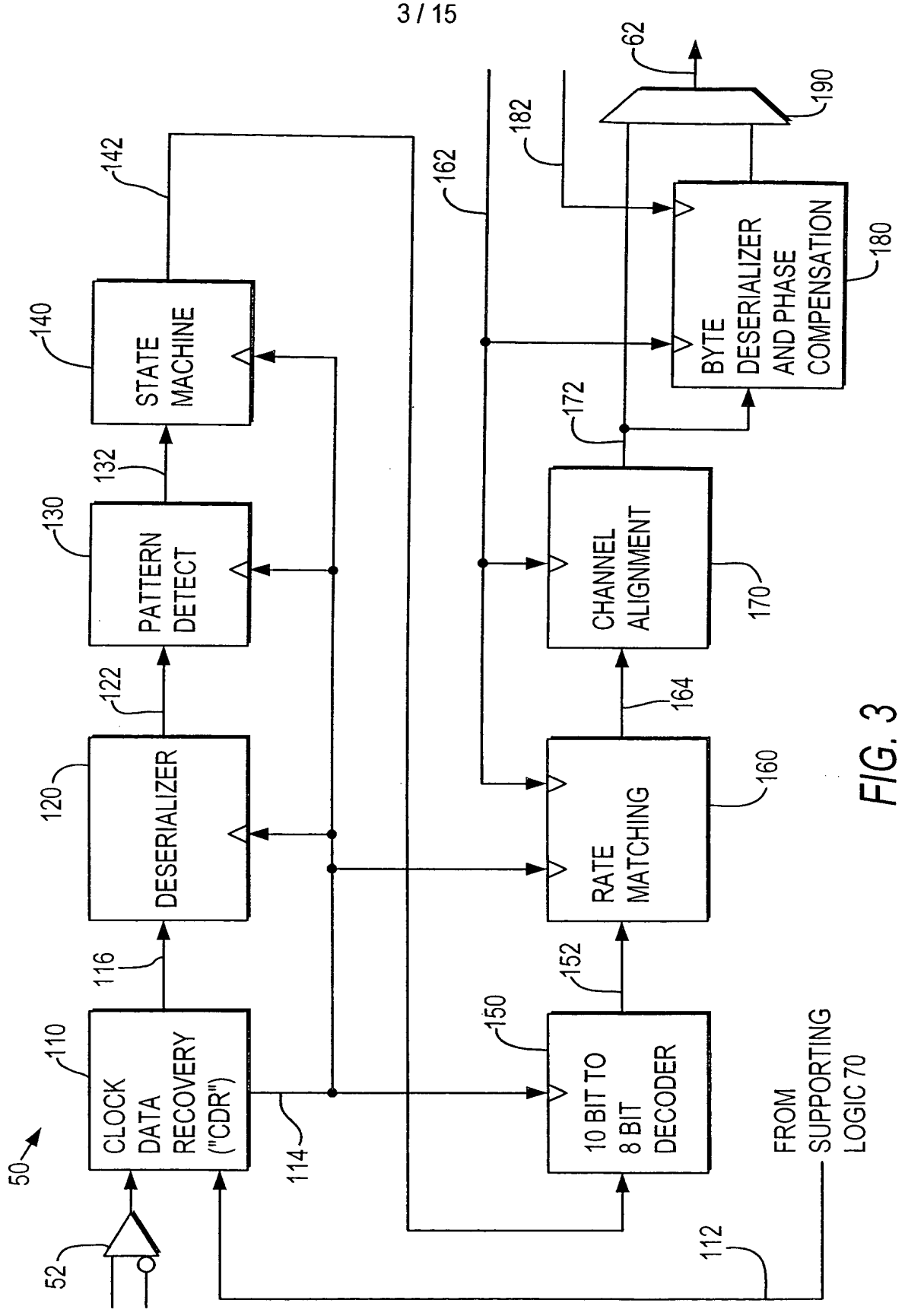

50
52
CLOCK DATA RECOVERY ("CDR")
110
114
116
DESERIALIZER
120
122
PATTERN DETECT
130
132
STATE MACHINE
140
142
10 BIT TO 8 BIT DECODER
150
152
RATE MATCHING
160
164
CHANNEL ALIGNMENT
170
172
BYTE DESERIALIZER AND PHASE COMPENSATION
180
182
190
62
112
162
FROM SUPPORTING LOGIC 70

FIG. 3

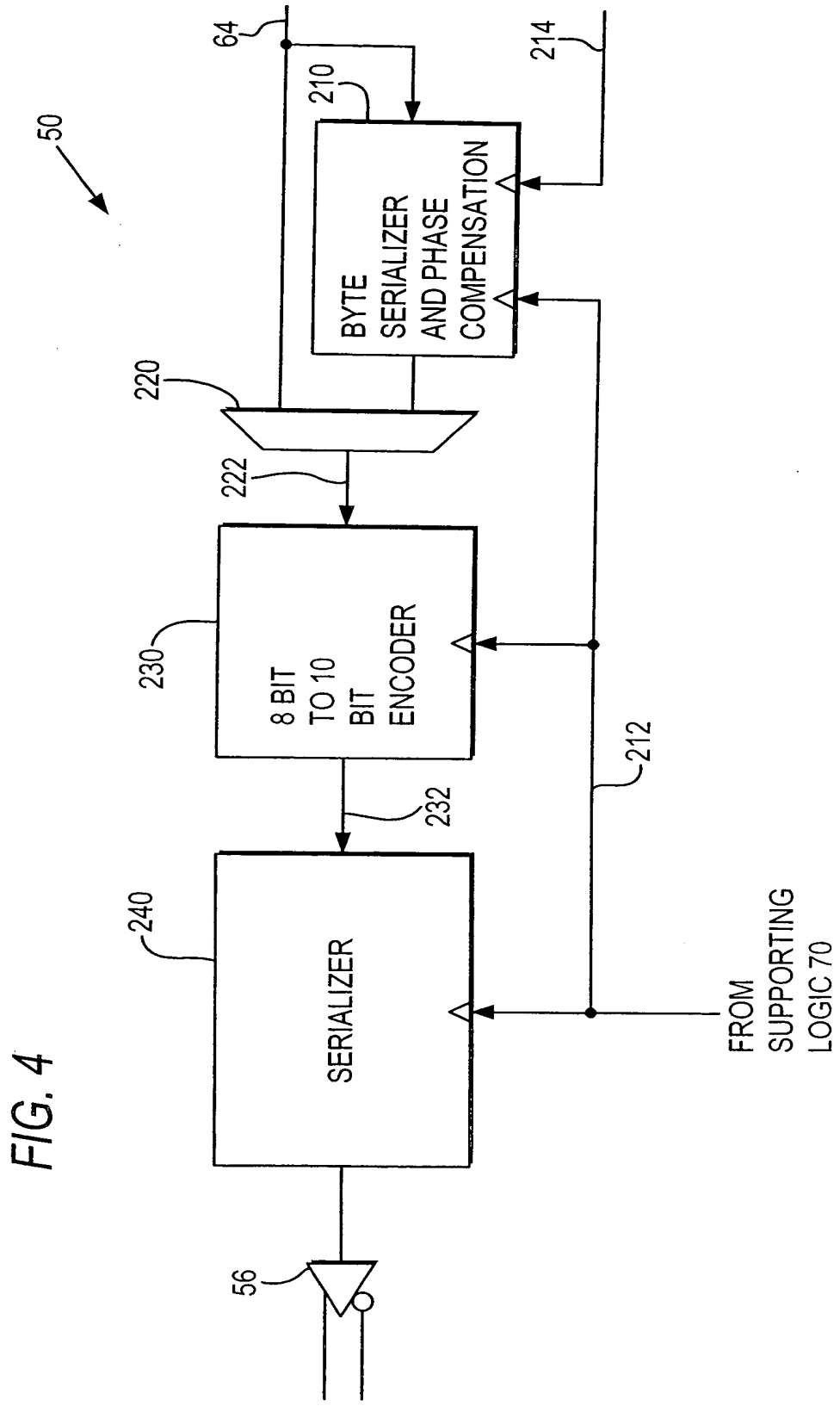

50
64
210
214
BYTE SERIALIZER AND PHASE COMPENSATION
220
222
230
8 BIT TO 10 BIT ENCODER
212
232
240
SERIALIZER
FROM SUPPORTING LOGIC 70
56

FIG. 4

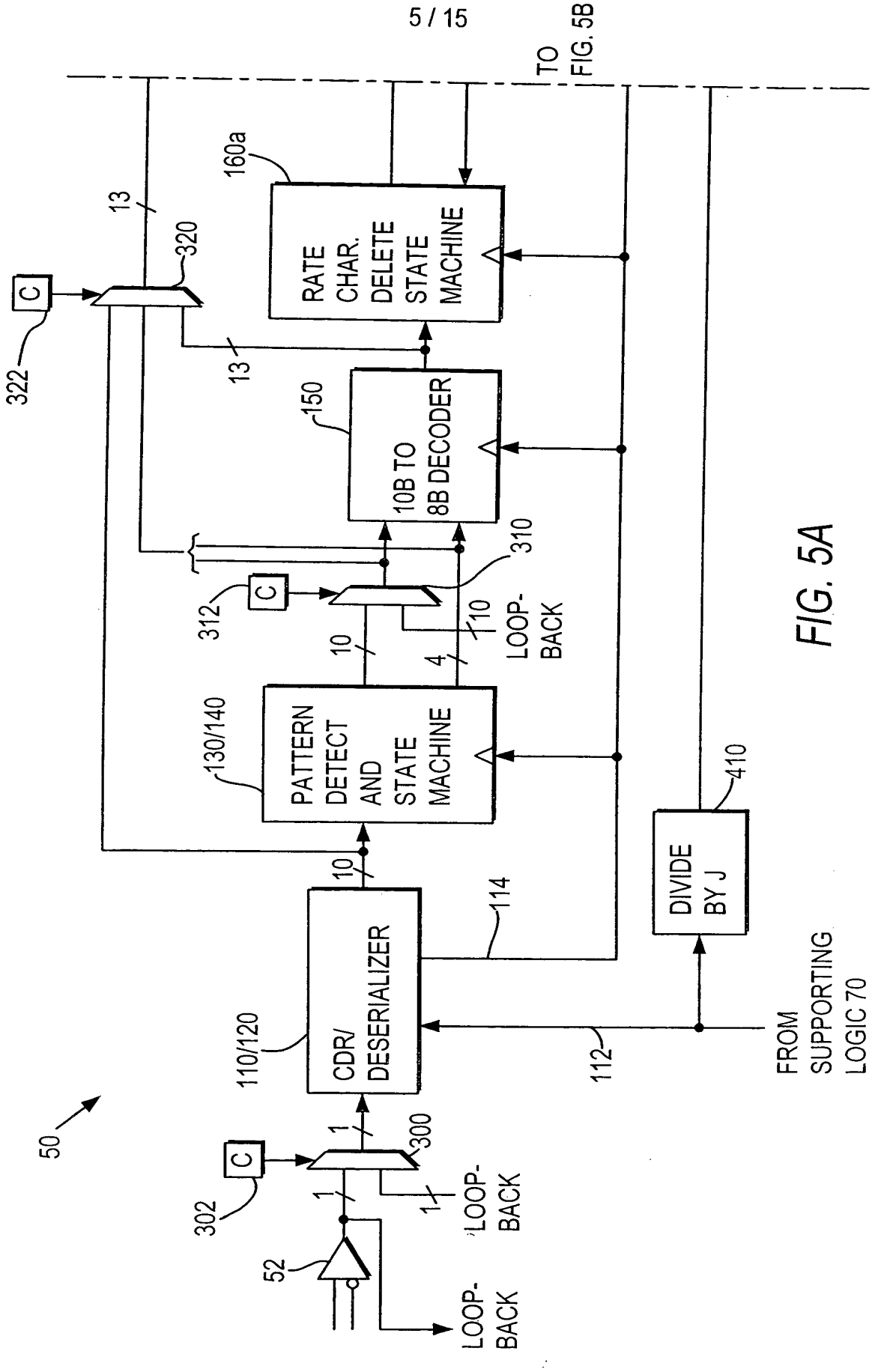
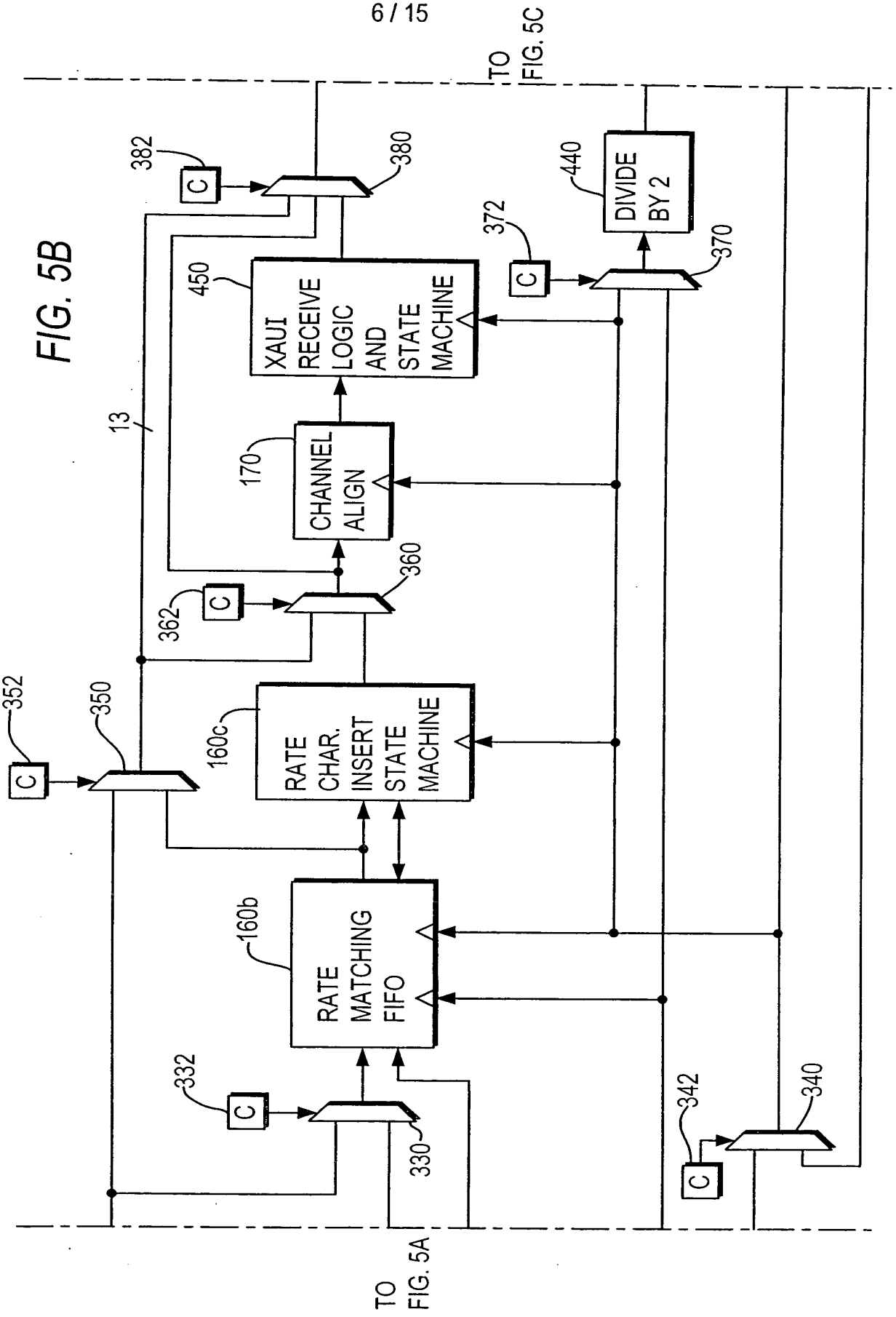

TO FIG. 5B
160a
RATE CHAR. DELETE STATE MACHINE
13
320
C
322
13
150
10B TO 8B DECODER
310
312
C
10
LOOP-BACK
10
4
130/140
PATTERN DETECT AND STATE MACHINE
410
DIVIDE BY J
10
114
110/120
CDR/ DESERIALIZER
112
FROM SUPPORTING LOGIC 70
50
1
300
C
302
1
1
LOOP-BACK
52
LOOP-BACK

FIG. 5A

FIG. 5B


TO FIG. 5C
382
C
380
440
DIVIDE BY 2
372
C
370
450
XAUI RECEIVE LOGIC AND STATE MACHINE
13
170
CHANNEL ALIGN
360
362
C
352
C
350
160c
RATE CHAR. INSERT STATE MACHINE
160b
RATE MATCHING FIFO
332
C
330
342
C
340
TO FIG. 5A

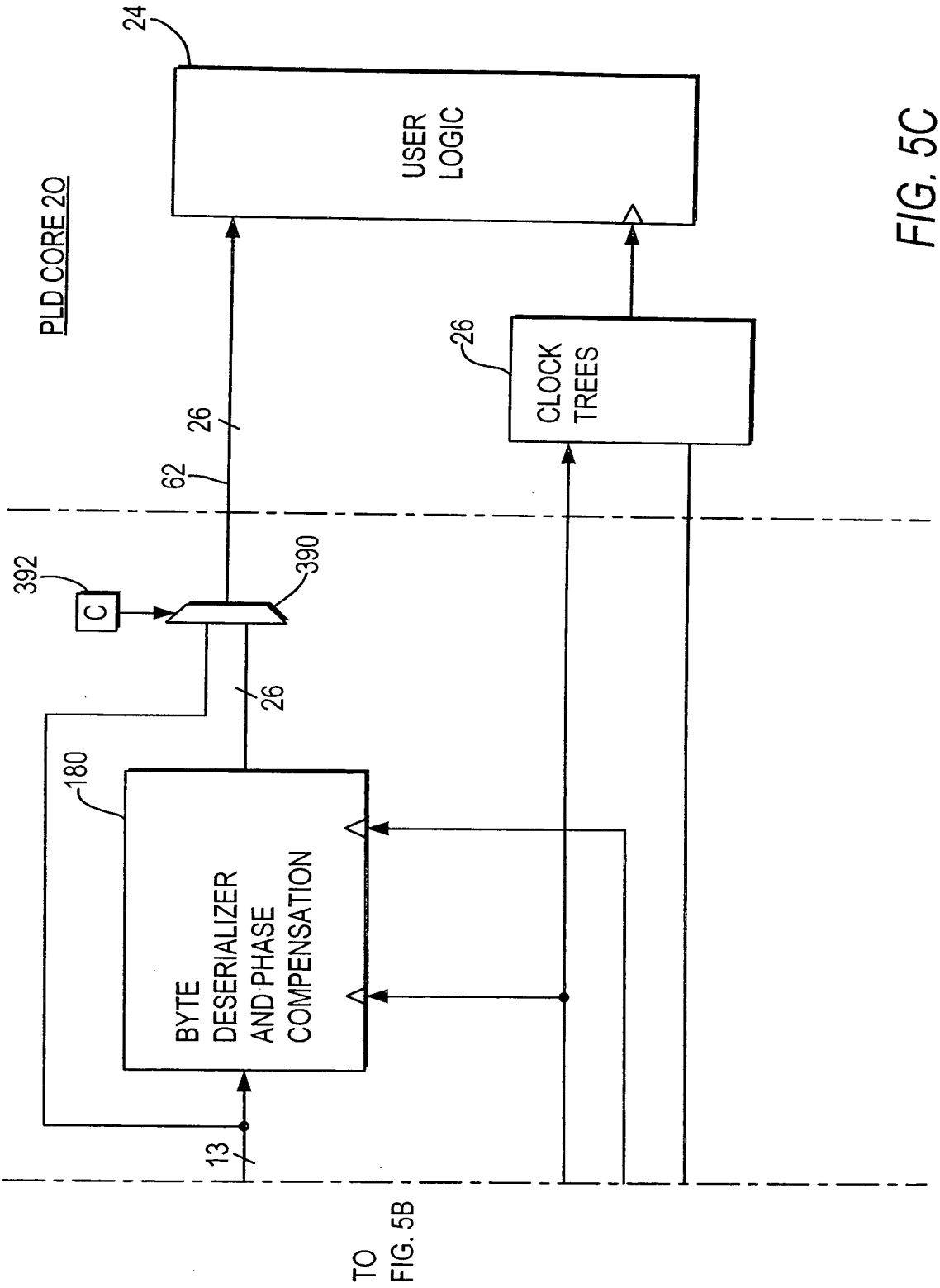

24
USER LOGIC
PLD CORE 20
26
CLOCK TREES
62
26
392
C
390
26
180
BYTE DESERIALIZER AND PHASE COMPENSATION
13
TO FIG. 5B

FIG. 5C

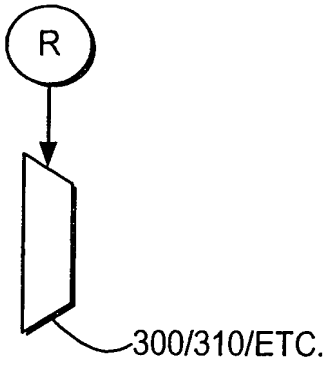


FIG. 6

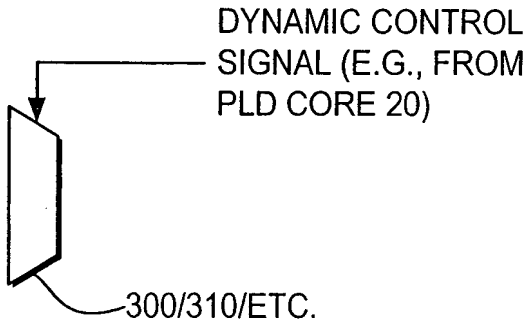


FIG. 7

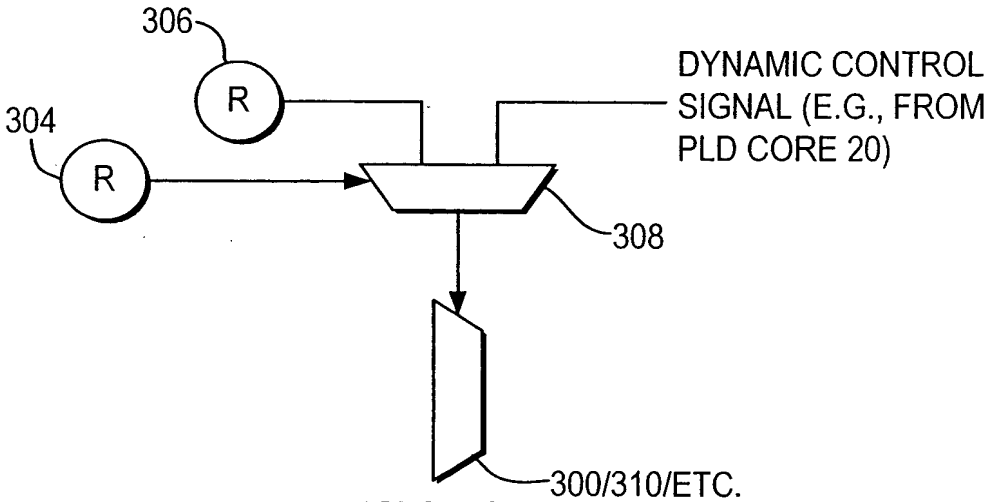


FIG. 8

FIG. 9

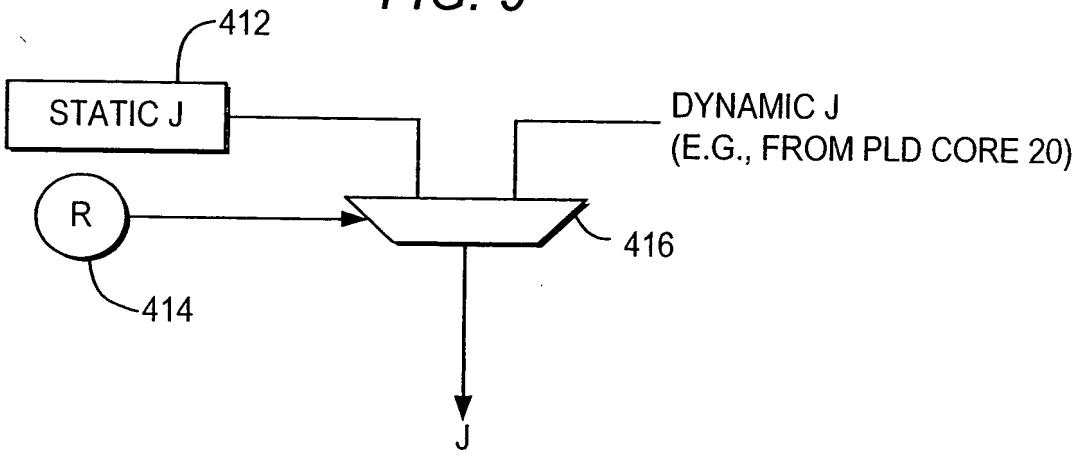

412
STATIC J
DYNAMIC J
(E.G., FROM PLD CORE 20)
R
416
414
J

FIG. 10

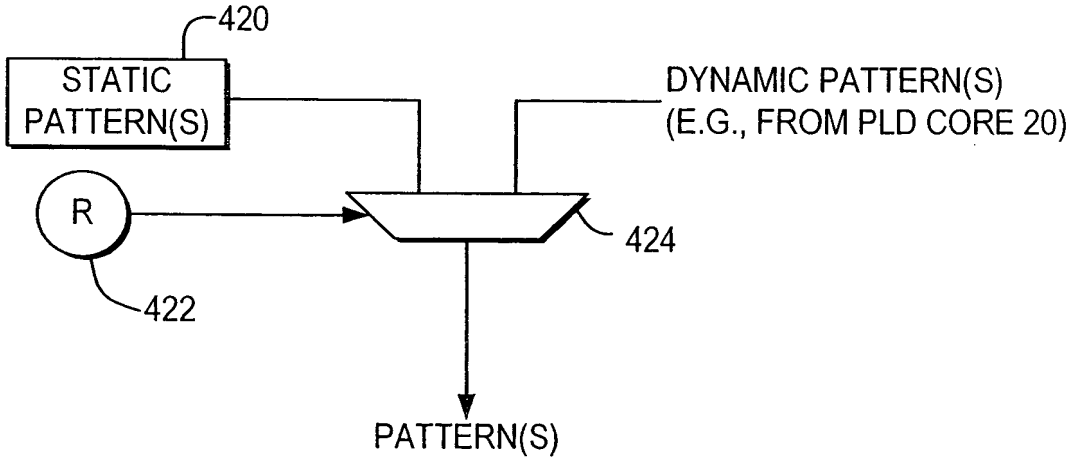
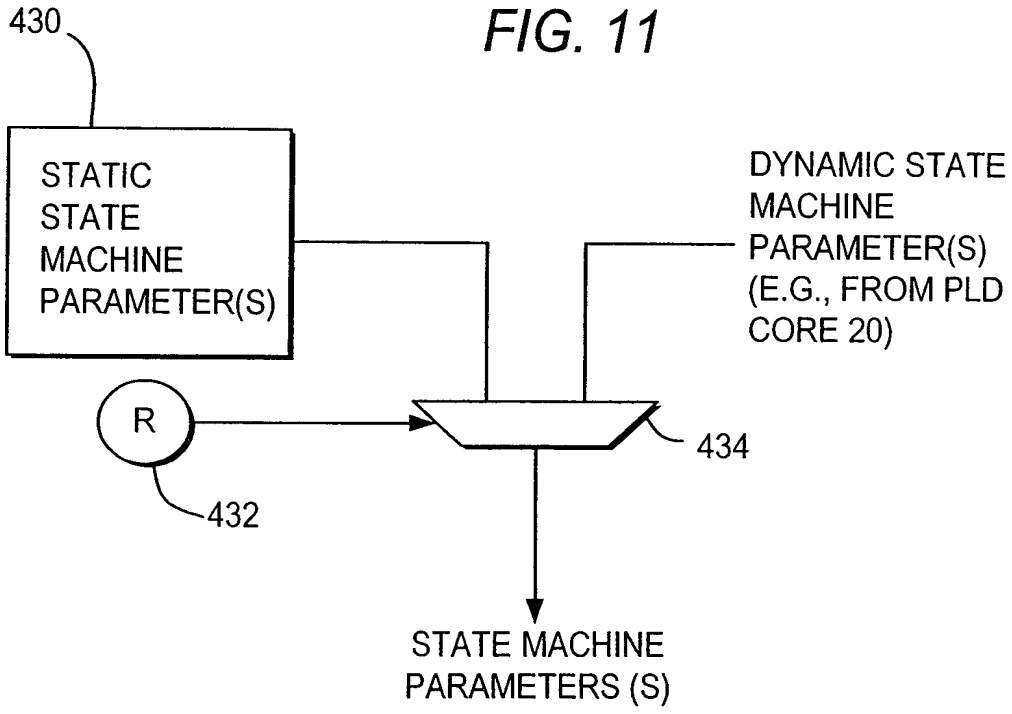

420
STATIC
PATTERN(S)
DYNAMIC PATTERN(S)
(E.G., FROM PLD CORE 20)
R
424
422
PATTERN(S)

FIG. 11


430
STATIC STATE MACHINE PARAMETER(S)
DYNAMIC STATE MACHINE PARAMETER(S) (E.G., FROM PLD CORE 20)
R
432
434
STATE MACHINE PARAMETERS (S)

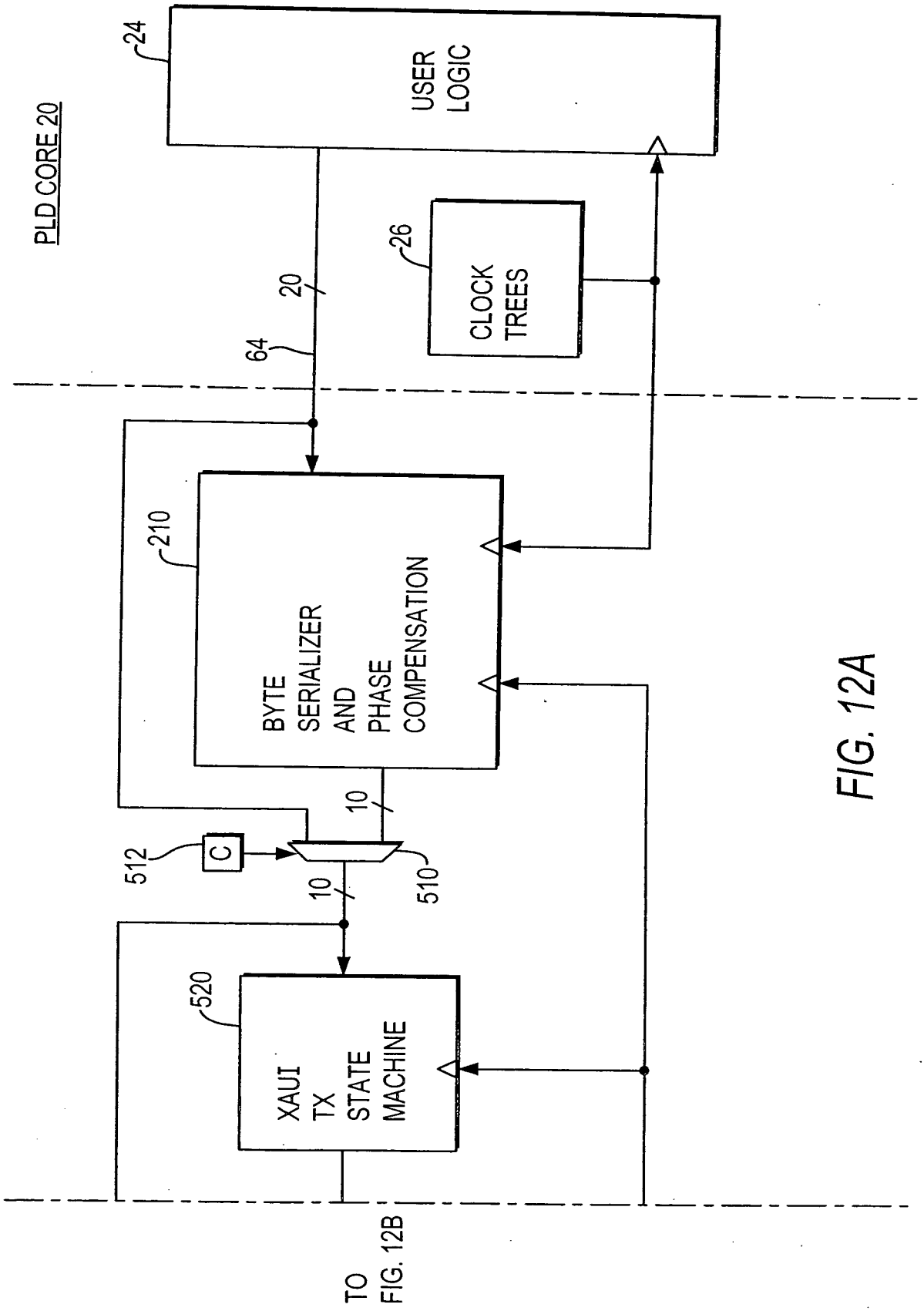

PLD CORE 20
24
USER LOGIC
26
CLOCK TREES
20
64
210
BYTE SERIALIZER AND PHASE COMPENSATION
10
512
C
10
510
520
XAUI TX STATE MACHINE
TO FIG. 12B

FIG. 12A

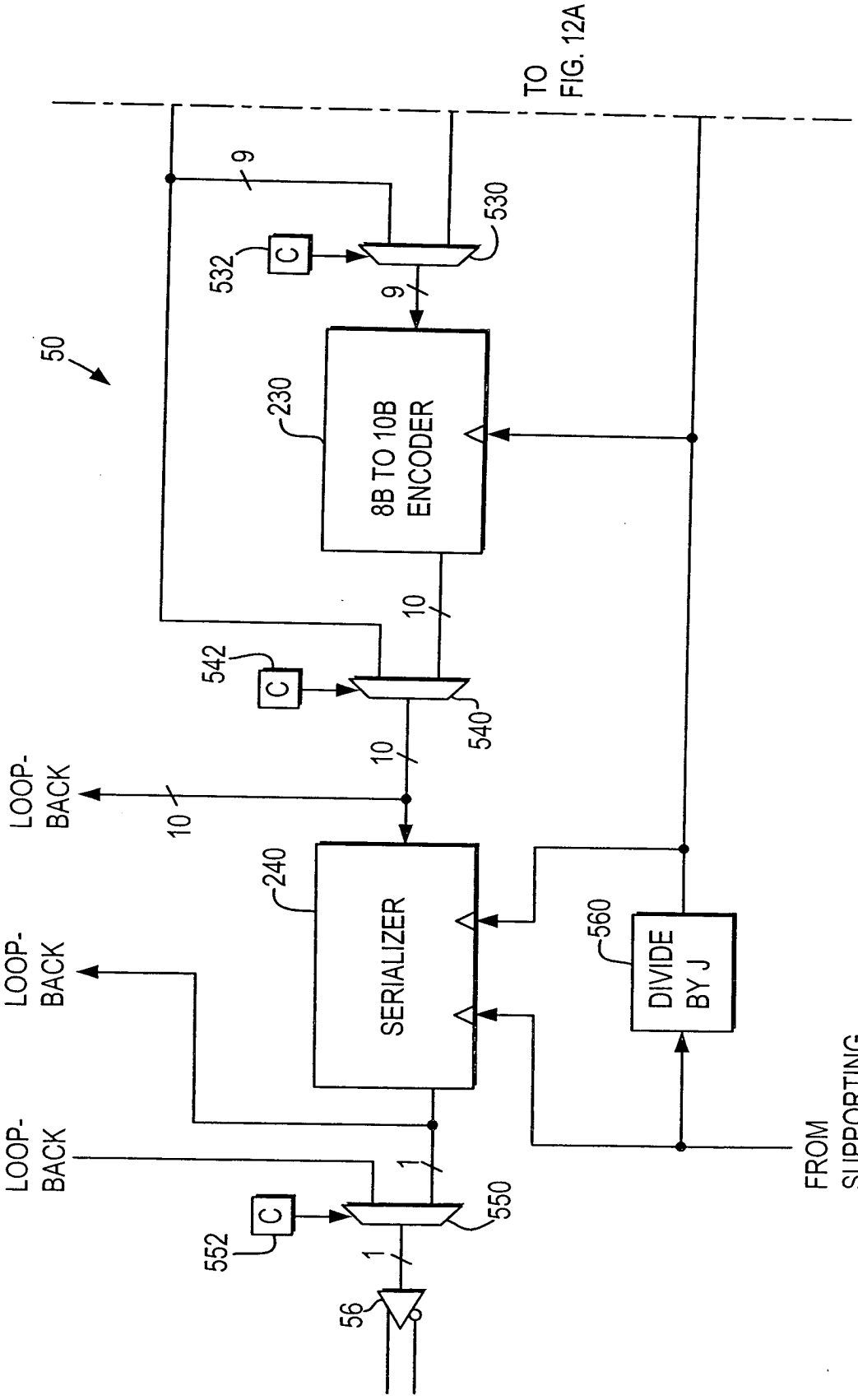

TO FIG. 12A
50
9
530
532
C
9
230
8B TO 10B ENCODER
10
542
C
540
10
LOOP-BACK
10
240
SERIALIZER
560
DIVIDE BY J
LOOP-BACK
LOOP-BACK
FROM SUPPORTING LOGIC 70
1
550
552
C
1
56

FIG. 12B

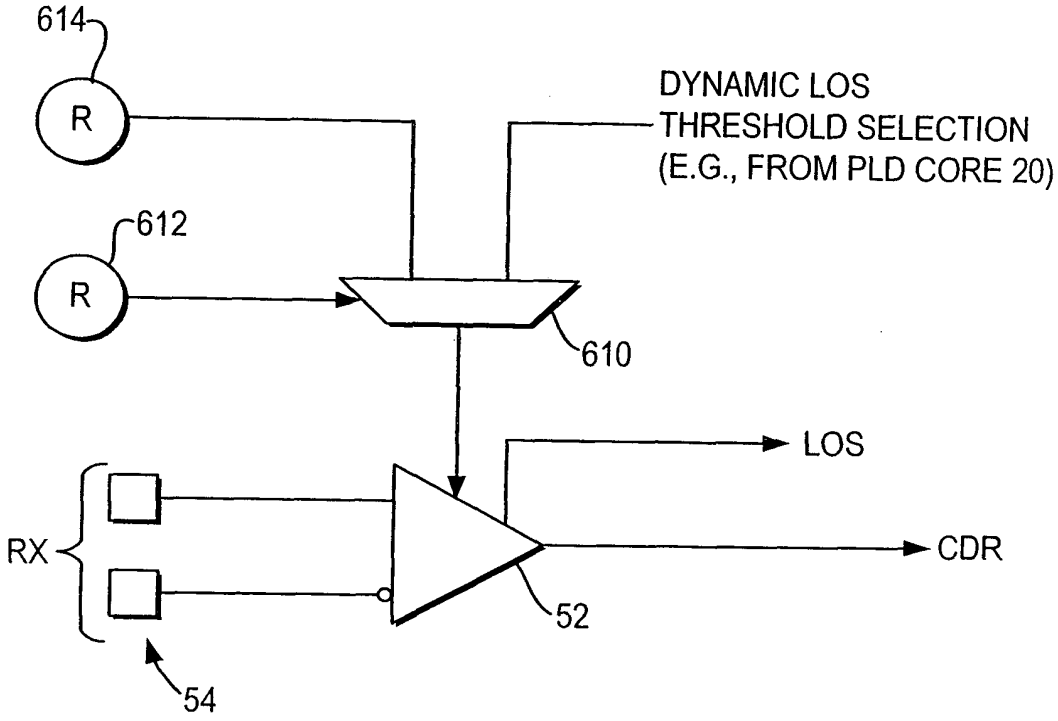

614
R
DYNAMIC LOS
THRESHOLD SELECTION
(E.G., FROM PLD CORE 20)
612
R
610
LOS
RX
CDR
52
54

FIG. 13

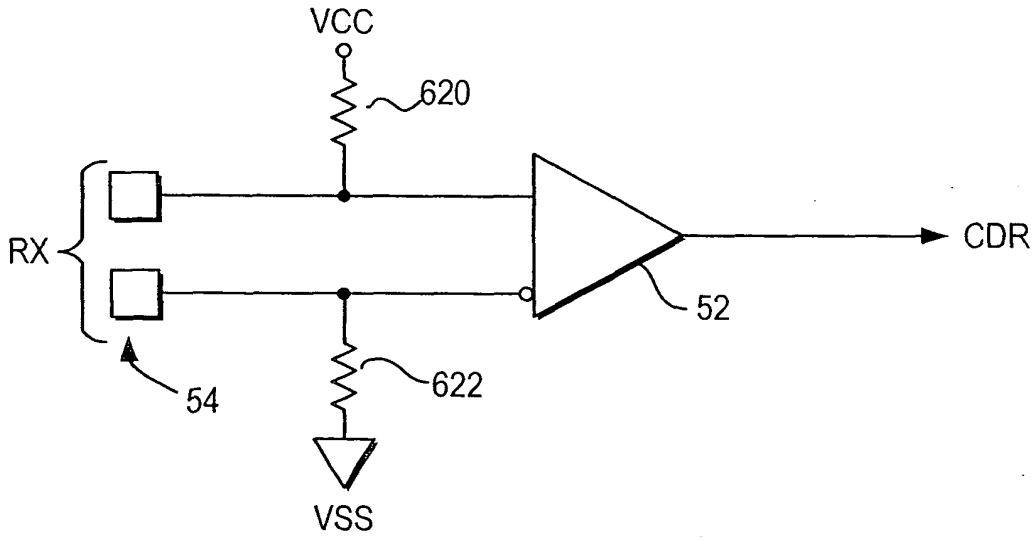

VCC
620
RX
CDR
52
54
622
VSS

FIG. 14

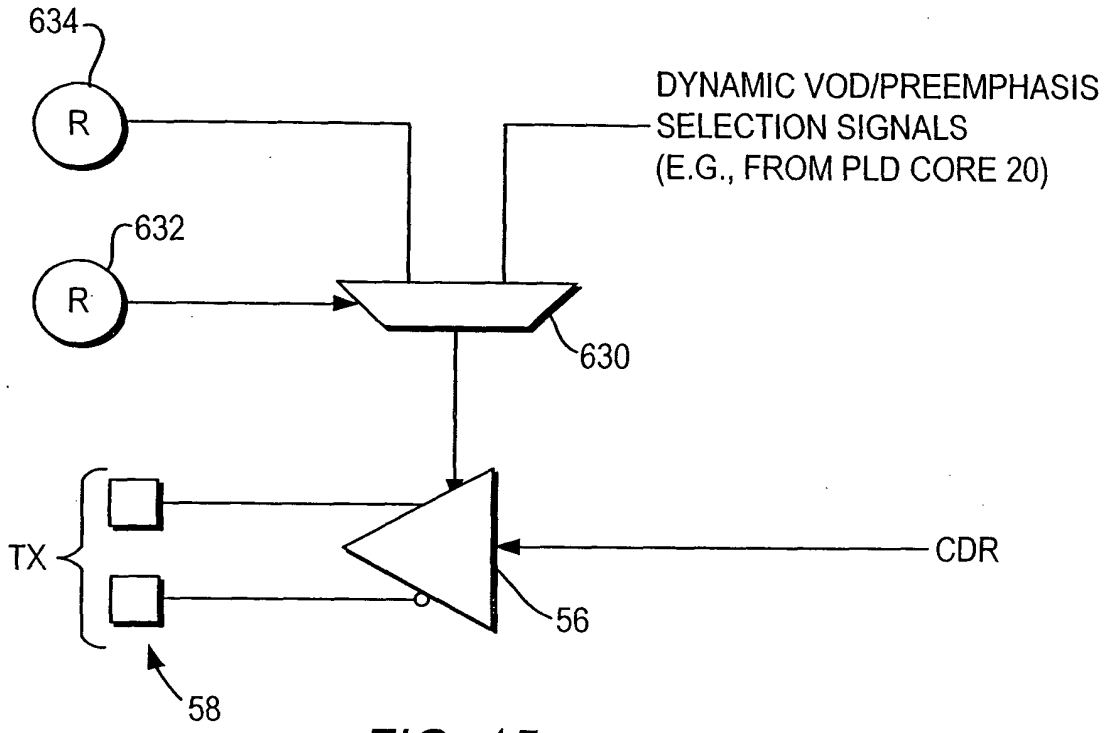

634
R
DYNAMIC VOD/PREEMPHASIS
SELECTION SIGNALS
(E.G., FROM PLD CORE 20)
632
R
630
TX
CDR
56
58

FIG. 15

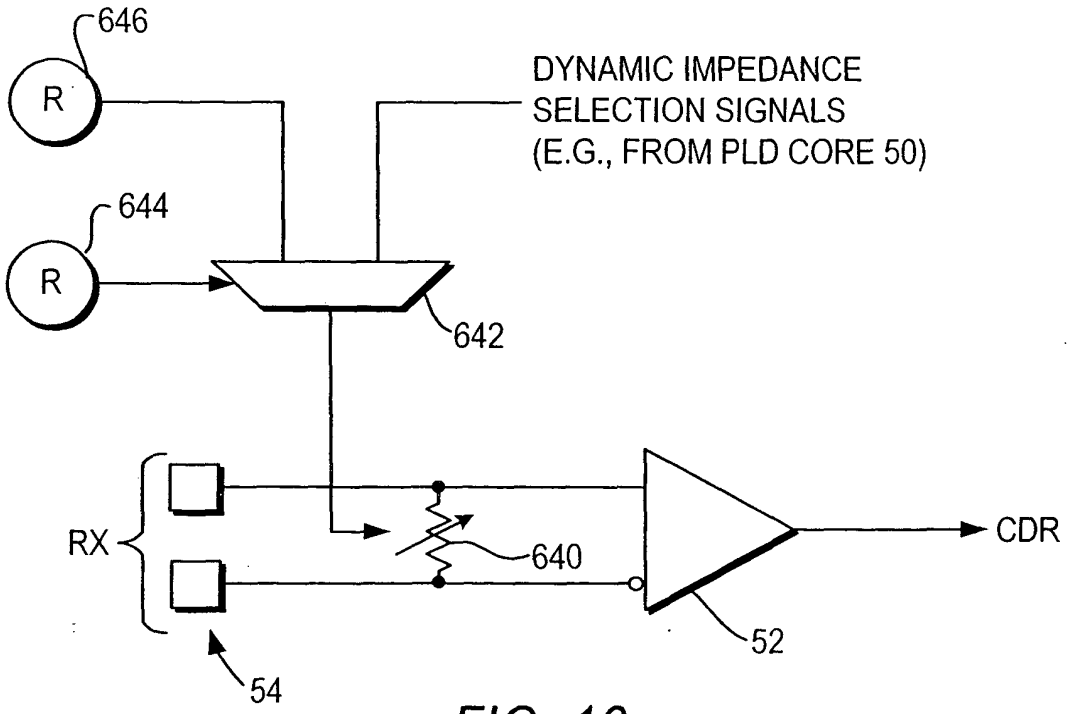
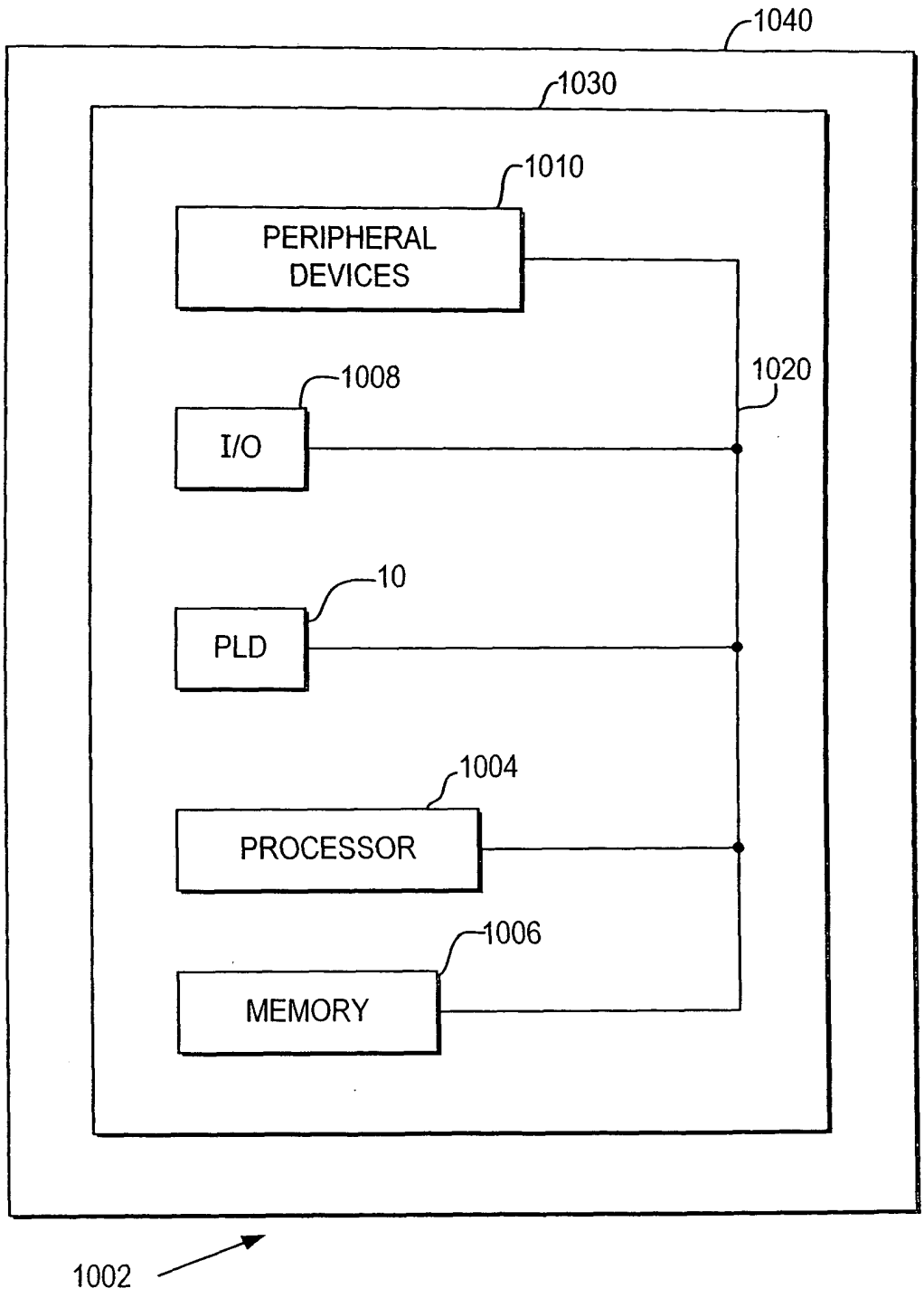

646
R
DYNAMIC IMPEDANCE
SELECTION SIGNALS
(E.G., FROM PLD CORE 50)
644
R
642
RX
640
CDR
52
54

FIG. 16

FIG. 17


1040
1030
1010
PERIPHERAL DEVICES
1020
1008
I/O
10
PLD
1004
PROCESSOR
1006
MEMORY
1002